DATA SHEET

SAA9750H
Camera Digital Signal Processor (CAMDSP)

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Camera Digital Signal Processor (CAMDSP)

SAA9750H

FEATURES

- Y/C separator for mosaic filter colour CCD which can be used with PAL or NTSC CCDs with horizontal resolution of 510, 670, 720 or 768 pixels
- Line sequential colour processing (R–Y) and (B–Y)
- 9 bit input signal (the internal processing is 10-bit)
- Digital feedback clamp control for Y/C separation
- Two 768 × 9 line memories for Y/C separation
- Aperture correction using phase linear filters
- Coring of LOW level signals to reduce noise
- Colour encoder in accordance with the PAL or NTSC system. Colour subcarrier is made by a discrete time oscillator (DTO) operating on system clock
- Slew rate controlled outputs for reduction of digital noise
- RGB inputs for title mix
- High accuracy 8 bit DAC outputs for luminance and chrominance signals
- Sync Signal Generator (SSG) to generate all necessary timing signals
- Serial interface for microprocessor control of CAMDSP settings
- Y and C signals accessible to incorporate digital features
- Including digital feature functions (mosaic, sepia, solarization, slice and negative/positive inversion).

GENERAL DESCRIPTION

The Camera Digital Signal Processor (CAMDSP) is intended for use with a mosaic filter colour CCD. The IC generates luminance and chrominance signals from the CCD signal. The device consists of a luminance and colour separator employing two 768 × 9 line memories, a PAL/NTSC encoder, a dual 8-bit video DAC, a Sync Signal Generator (SSG) and a simple serial interface to control many settings.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA1}	Y-DAC analog supply voltage (pin 1)	2.7	3.0	3.3	V
V_{DDA2}	C-DAC analog supply voltage (pin 2)	2.7	3.0	3.3	V
V_{DDD1}	digital supply voltage (pin 41)	2.7	3.0	3.3	V
V_{DDD2}	digital supply voltage (pin 53)	2.7	3.0	3.3	V
V_{DDD3}	digital supply voltage (pin 65)	2.7	3.0	3.3	V
V_{IH}	HIGH level digital input voltage	$0.7V_{DDD}$	–	V_{DDD}	V
V_{IL}	LOW level digital input voltage	0	–	$0.3V_{DDD}$	V
V_{OH}	HIGH level digital output voltage	$V_{DDD} - 0.5$	–	–	V
V_{OL}	LOW level digital output voltage	–	–	0.5	V
T_{amb}	operating ambient temperature	–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA9750H	LQFP80	plastic low profile quad flat package; 80 leads; body 12 × 12 × 1.4 mm	SOT315-1

BLOCK DIAGRAM

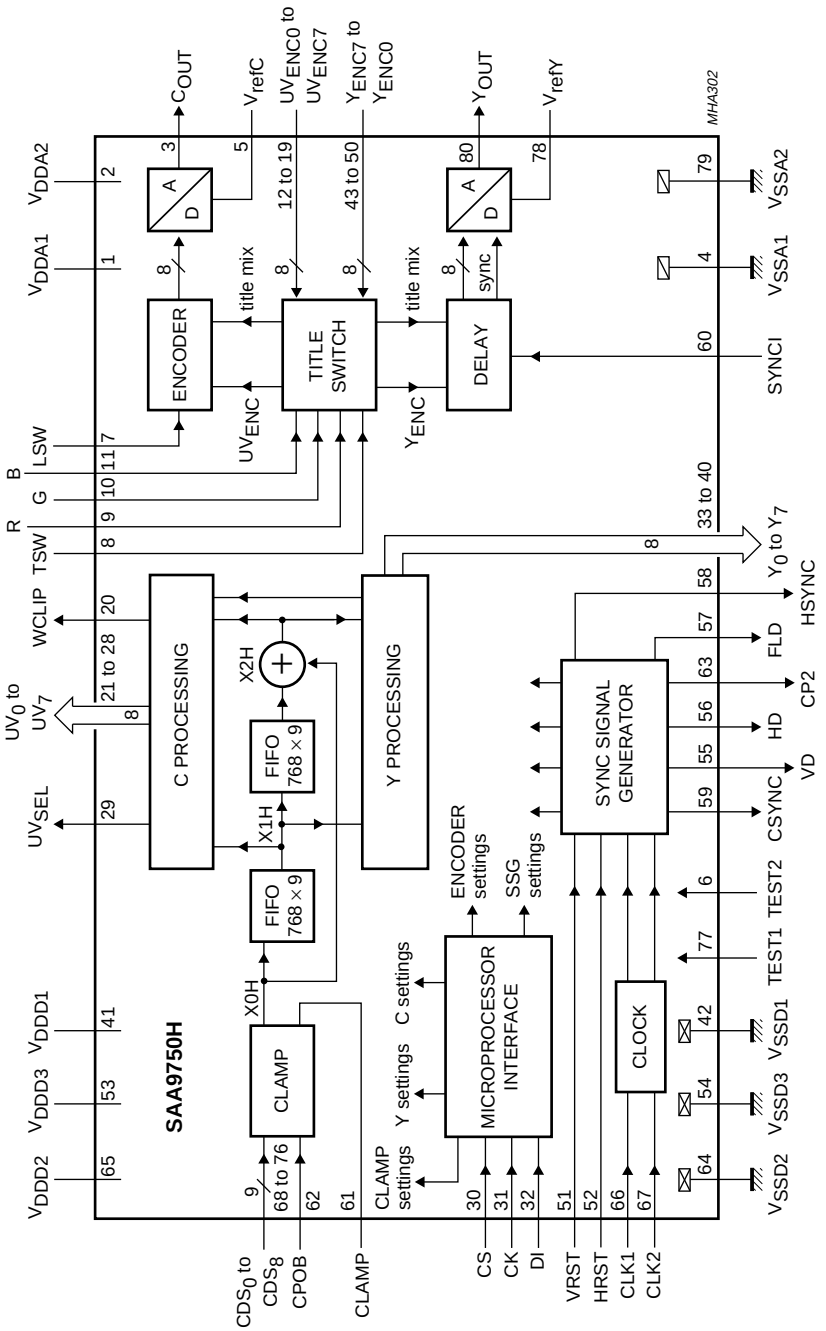


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	INPUT/OUTPUT	ANALOG/DIGITAL	DESCRIPTION
V_{DDA1}	1	supply	–	analog supply voltage 1 for Y-DAC
V_{DDA2}	2	supply	–	analog supply voltage 2 for C-DAC
C_{OUT}	3	output	analog	C-DAC output
V_{SSA1}	4	supply	–	analog ground 1 for C-DAC
V_{refC}	5	–	–	C-DAC decoupling voltage
TEST2	6	input	digital	test 2 pin
LSW	7	input	digital	line switch for SECAM
TSW	8	input	digital	title memory switch
R	9	input	digital	title memory colour (red)
G	10	input	digital	title memory colour (green)
B	11	input	digital	title memory colour (blue)
UV_{ENC0}	12	input	digital	B–Y and R–Y signal to encoder (LSB)
UV_{ENC1}	13	input	digital	B–Y and R–Y signal to encoder
UV_{ENC2}	14	input	digital	B–Y and R–Y signal to encoder
UV_{ENC3}	15	input	digital	B–Y and R–Y signal to encoder
UV_{ENC4}	16	input	digital	B–Y and R–Y signal to encoder
UV_{ENC5}	17	input	digital	B–Y and R–Y signal to encoder
UV_{ENC6}	18	input	digital	B–Y and R–Y signal to encoder
UV_{ENC7}	19	input	digital	B–Y and R–Y signal to encoder (MSB)
WCLIP	20	output	digital	white-clip
UV_7	21	output	digital	time multiplexed B–Y and R–Y (MSB)
UV_6	22	output	digital	time multiplexed B–Y and R–Y
UV_5	23	output	digital	time multiplexed B–Y and R–Y
UV_4	24	output	digital	time multiplexed B–Y and R–Y
UV_3	25	output	digital	time multiplexed B–Y and R–Y
UV_2	26	output	digital	time multiplexed B–Y and R–Y
UV_1	27	output	digital	time multiplexed B–Y and R–Y
UV_0	28	output	digital	time multiplexed B–Y and R–Y (LSB)
UV_{SEL}	29	output	digital	B–Y or R–Y active at UV output
CS	30	input	digital	microprocessor interface (chip select)
CK	31	input	digital	microprocessor interface (clock)
DI	32	input	digital	microprocessor interface (data input)
Y_0	33	output	digital	luminance signal (LSB)
Y_1	34	output	digital	luminance signal
Y_2	35	output	digital	luminance signal
Y_3	36	output	digital	luminance signal
Y_4	37	output	digital	luminance signal
Y_5	38	output	digital	luminance signal
Y_6	39	output	digital	luminance signal
Y_7	40	output	digital	luminance signal (MSB)

SYMBOL	PIN	INPUT/OUTPUT	ANALOG/DIGITAL	DESCRIPTION
V_{DDD1}	41	supply	–	digital supply voltage 1
V_{SSD1}	42	supply	–	digital ground 1
Y_{ENC7}	43	input	digital	luminance signal to encoder (MSB)
Y_{ENC6}	44	input	digital	luminance signal to encoder
Y_{ENC5}	45	input	digital	luminance signal to encoder
Y_{ENC4}	46	input	digital	luminance signal to encoder
Y_{ENC3}	47	input	digital	luminance signal to encoder
Y_{ENC2}	48	input	digital	luminance signal to encoder
Y_{ENC1}	49	input	digital	luminance signal to encoder
Y_{ENC0}	50	input	digital	luminance signal to encoder (LSB)
VRST	51	input	digital	external VD (vertical drive)
HRST	52	input	digital	external HD (horizontal drive)
V_{DDD3}	53	supply	–	digital supply voltage 3
V_{SSD3}	54	supply	–	digital ground 3
VD	55	output	digital	VD timing for PPG IC
HD	56	output	digital	HD timing for PPG IC
FLD	57	output	digital	field pulse output
HSYNC	58	output	digital	horizontal timing for YC processing
CSYNC	59	output	digital	composite sync pulse
SYNCI	60	input	digital	sync input for bypass mode
CLAMP	61	output (3-state)	digital	clamp voltage control
CPOB	62	input	digital	optical black pulse
CP2	63	output	digital	clamping pulse
V_{SSD2}	64	supply	–	digital ground 2
V_{DDD2}	65	supply	–	digital supply voltage 2
CLK1	66	input	digital	clock 1
CLK2	67	input	digital	clock 2
CDS_0	68	input	digital	CDS signal (LSB)
CDS_1	69	input	digital	CDS signal
CDS_2	70	input	digital	CDS signal
CDS_3	71	input	digital	CDS signal
CDS_4	72	input	digital	CDS signal
CDS_5	73	input	digital	CDS signal
CDS_6	74	input	digital	CDS signal
CDS_7	75	input	digital	CDS signal
CDS_8	76	input	digital	CDS signal (MSB)
TEST1	77	input	digital	test 1 pin
V_{refY}	78	–	–	Y-DAC decoupling voltage
V_{SSA2}	79	supply	–	analog ground 2 for Y-DAC
Y_{OUT}	80	output	analog	Y-DAC output

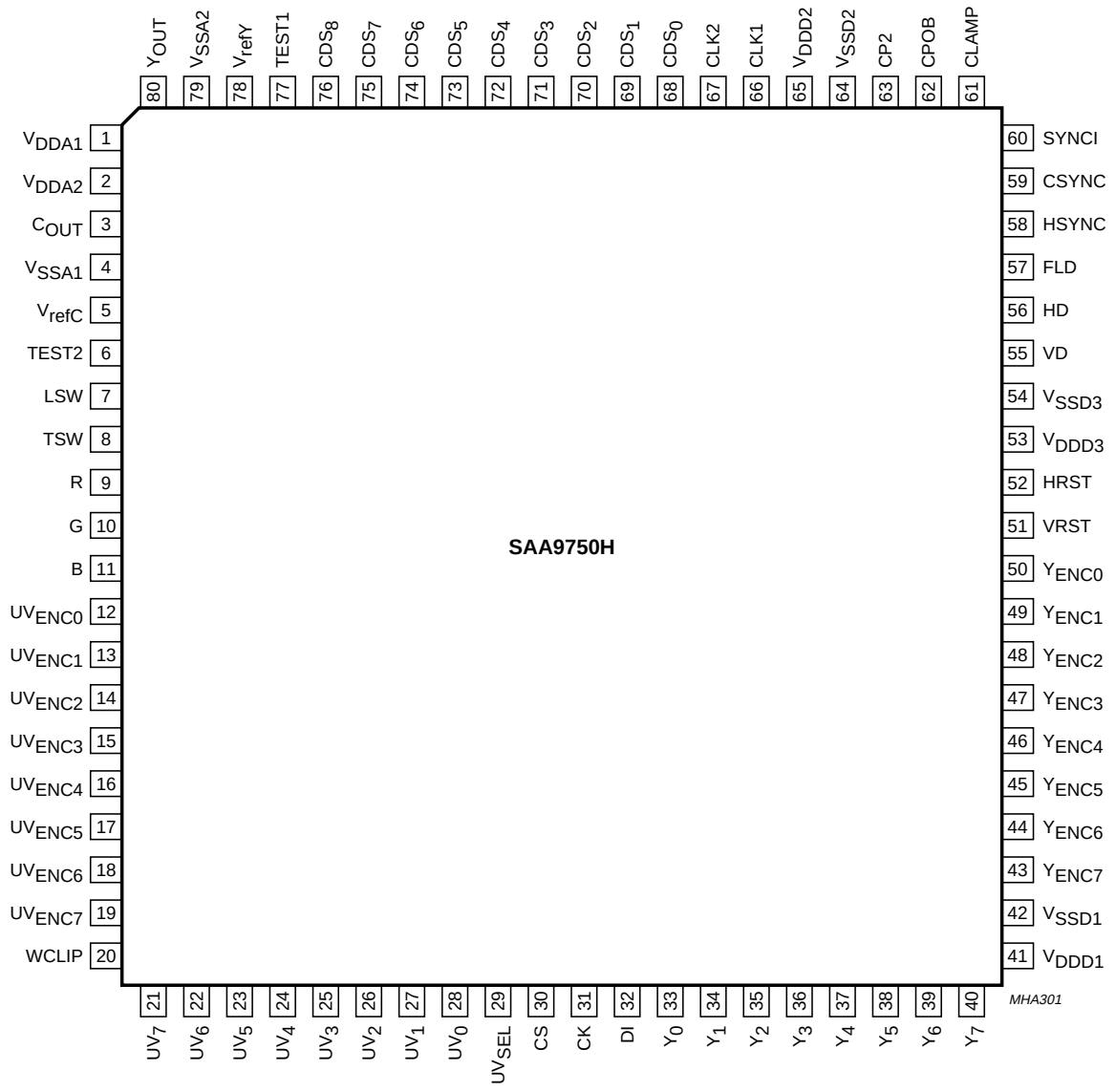


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The Camera Digital Signal Processor (CAMDSP) is intended for use with a mosaic filter colour CCD.

The input signal is an 8-bit or 9-bit digitized CCD signal.

After AGC and gamma correction, clamping of the input signal is achieved by feedback clamp level control.

In the luminance processing, symmetrical horizontal and vertical aperture correction are carried out. Coring is also carried out to reduce noise at LOW signal levels. In the chrominance processing, white balance control and matrix control is adjustable. A false colour correction circuit reduces aliasing of high frequency input signals.
A white-clip makes the colour white at highlights.

In the encoder part, the colour encoder subcarrier is made by the discrete time oscillator thus eliminating the use of an extra crystal. The subcarrier frequency for PAL or NTSC is selectable. The encoding can be in PAL or NTSC format.

The encoded signal is output via separate 8-bit digital-to-analog converters (DACs) for luminance and chrominance. In the event of SECAM the output is a line sequential –(R–Y)/(B–Y) signal. A line memory interface allows for mixing of RGB signals in the main signal.
The encoder can be bypassed completely, in this event only the title mix is carried out before digital-to-analog conversion.

The SSG generates all necessary timing signals. Timing signals for external devices NTSC, PAL and SECAM are also made. The SSG can be locked to an external video source.

CAMDSP can operate with 510H, 670H, 720H and 768H colour mosaic CCDs both PAL and NTSC type. In the 510H CCD application the upsampling clock is used for the encoder part, therefore two clock frequencies (f_s and $2f_s$) are required.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.5	+5.0	V
V_{DDA}	analog supply voltage		–0.5	+5.0	V
P_{tot}	total power dissipation		–	500	mW
V_I	digital input voltage		–0.5	V_{DDD} + 0.5	V
V_O	digital output voltage		–0.5	V_{DDD} + 0.5	V
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	operating ambient temperature		–20	+70	°C
V_{es}	electrostatic handling	note 1	–2000	+2000	V
I_{latch}	latch-up protection current		100	–	mA

Note

1. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	57	K/W

DC CHARACTERISTICS

V_{DD} = 2.7 to 3.3 V; T_{amb} = –20 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DD}	supply current	note 1	–	60	150	mA
Inputs: LSW, TSW, R, G, B, UV_{ENC0} to UV_{ENC7}, CS, CK, DI, Y_{ENC0} to Y_{ENC7}, VRST, HRST, SYNCI, CPOB, CLK1, CLK2, CDS_0 to CDS_7, TEST1 and TEST2						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
I_{IH}	HIGH level input current	$V_{IH} = V_{DD}$	–	–	1	µA
I_{IL}	LOW level input current	$V_{IL} = V_{SS}$	–	–	–1	µA
Outputs: WCLIP, UV_0 to UV_7, UV_{SEL}, Y_0 to Y_7, VD, HD, FLD, HSYNC, CSYNC and CP2						
V_{OH}	HIGH level output voltage	I_{OH} = –20 µA	V_{DD} – 0.1	–	–	V
		I_{OH} = –2 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{OL} = +20 µA	–	–	0.1	V
		I_{OL} = +2 mA	–	–	0.5	V
Output: CLAMP (3-state output)						
V_{OH}	HIGH level output voltage	I_{OH} = –20 µA	V_{DD} – 0.1	–	–	V
		I_{OH} = –8 mA	V_{DD} – 0.5	–	–	V
V_{OL}	LOW level output voltage	I_{OL} = +20 µA	–	–	0.1	V
		I_{OL} = +8 mA	–	–	0.5	V
I_{TL}	3-state leakage current	$V_{IH} = V_{DD}$; $V_{IL} = V_{SS}$	–	–	±5	µA

Note

1. 510H PAL; V_{DD} = 3 V; DAC R_L = 2 kΩ.

DAC CHARACTERISTICS

V_{DD} = 3.0 V; T_{amb} = +25 °C; R_L = open-circuit; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Outputs: Y_{OUT} and C_{OUT}					
f_{Cmax}	conversion frequency speed	20	–	–	MHz
INL	DC integral linearity error	–0.5	–	+0.5	LSB
DNL	DC differential linearity error	–0.5	–	+0.5	LSB
$V_{O(p-p)}$	full scale output except sync (peak-to-peak value)	1.61	1.66	1.72	V
R_O	internal series output resistance	–	75	–	Ω

AC CHARACTERISTICS

Microprocessor interface

V_{DD} = 2.7 to 3.3 V; V_{IL} = 0 V; $V_{IH} = V_{DD}$; $V_{ref} = 0.5V_{DD}$; T_{amb} = –20 to +70 °C; input t_r and t_f = 30 ns; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{CSs}	CS set-up time	0.4	–	–	µs
t_{CSh}	CS hold time	0.4	–	–	µs
t_{CSd}	CS deselection time	0.2	–	–	µs
t_{Ds}	DI set-up time	0.4	–	–	µs
t_{Dh}	DI hold time	0.4	–	–	µs
f_{CK}	CK frequency	–	–	0.5	MHz
t_{WCKH}	HIGH level pulse width of CK	1.0	–	–	µs
t_{WCKL}	LOW level pulse width of CK	1.0	–	–	µs
t_r	rise time of CK	–	–	100	ns
t_f	fall time of CK	–	–	100	ns

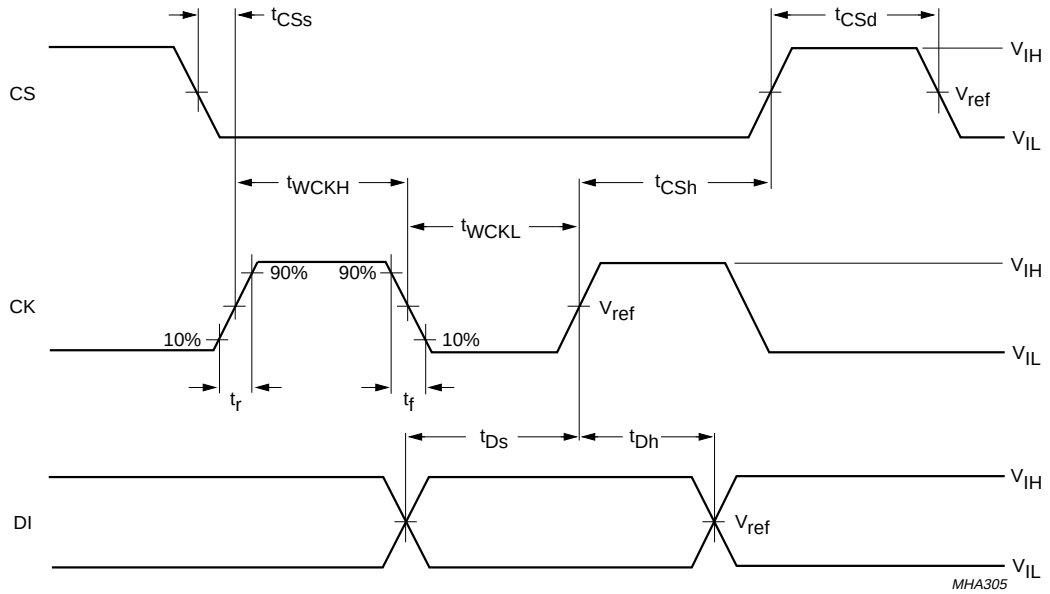


Fig.3 Microprocessor interface timing.

Data input/output timing (CLK1 and CLK2)

V_{DD} = 2.7 to 3.3 V; V_{IL} = 0 V; $V_{IH} = V_{DD}$; $V_{ref} = 0.5V_{DD}$;T_{amb} = −20 to +70 °C; t_r and t_f = 6 ns; output load capacitance = 20 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{DIs}	data input set-up time	note 1	5	–	–	ns
t_{DIh}	data input hold time	note 1	8	–	–	ns
t_{DOd}	data output delay time	notes 2 and 3	–	–	50	ns
t_{DOh}	data output hold time	notes 2 and 3	–	–	50	ns
t_{duty}	duty factor of CLK1 and CLK2		–	50	–	%

Notes

1. Data inputs: SYNCI, CPOB, CDS_0 to CDS_8, VRST, HRST, R, G, B, TSW, Y_{ENC0} to Y_{ENC7}, LSW and UV_{ENC0} to UV_{ENC7}.
2. Data outputs: UV_{SEL}, UV_0 to UV_7, Y_0 to Y_7, WCLIP, CSYNC, HSYNC, FLD, HD, VD and CP2.
3. T_{amb} = +25 °C; V_{DD} = 3.0 V.

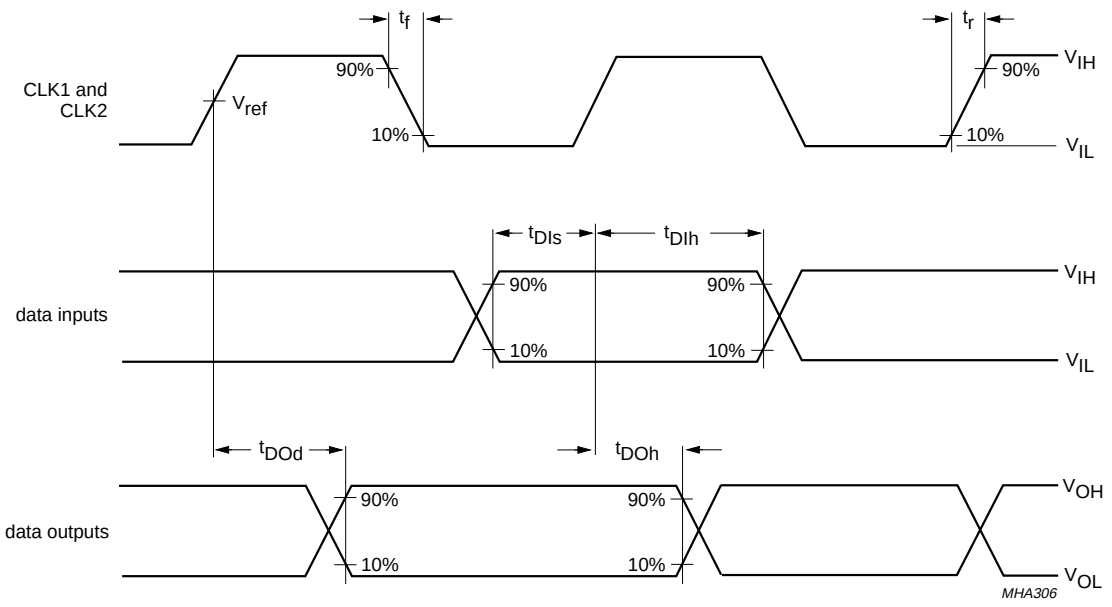


Fig.4 Data input/output timing (CLK1 and CLK2).

SSG TIMING

Clock count for NTSC and PAL mode

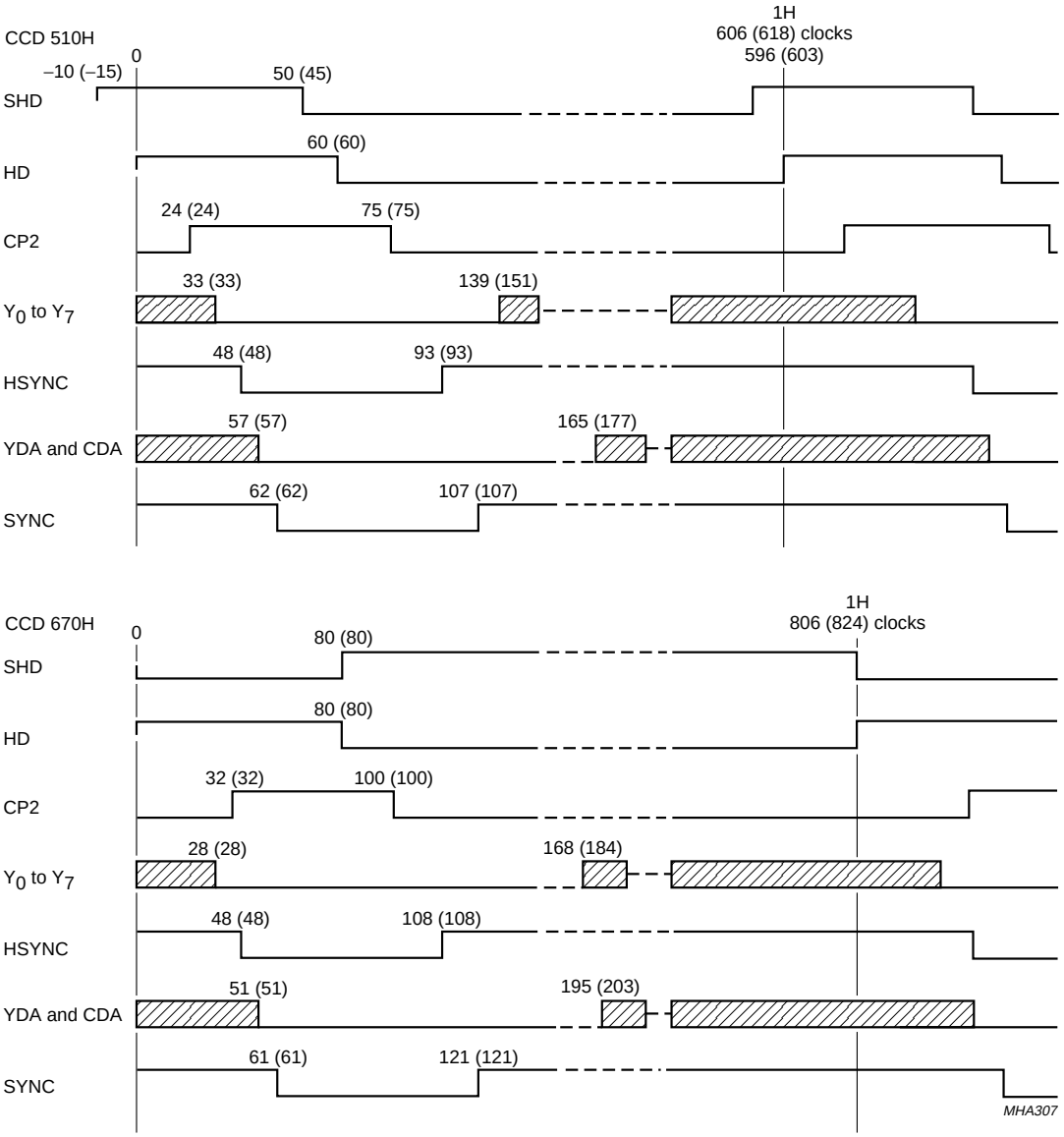


Fig.5 SSG timing (continued in Fig.6).

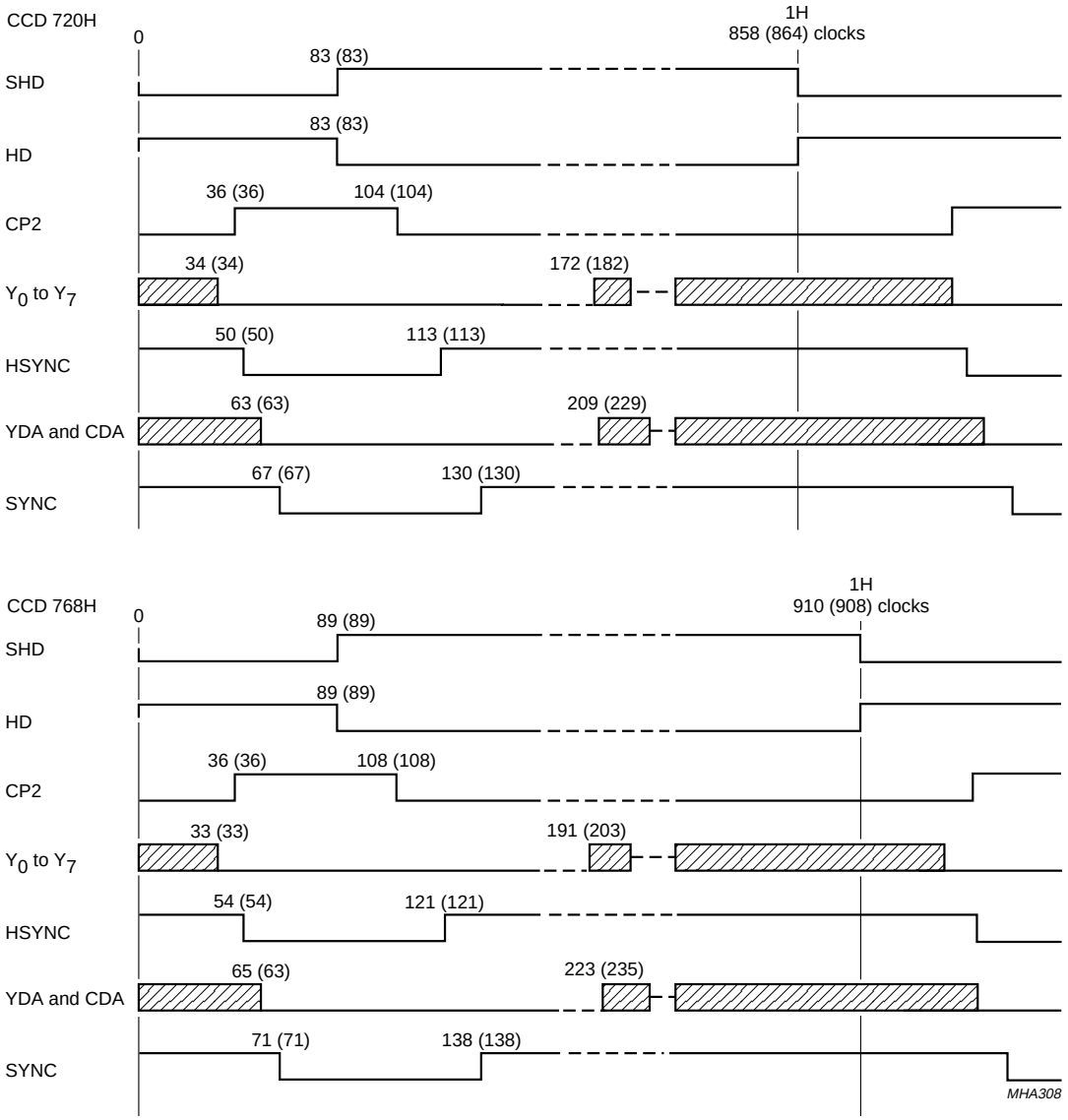


Fig.6 SSG timing (continued from Fig.5).

SHD: HD output can be changed by microprocessor to SHD outputs.
HD: For timing of input CDS signal for PPG IC.
HSYNC: For output luminance signal Y7 to Y0 and chrominance signal UV7 to UV0 of CAMDSPs YC processing.
SYNC: Composite SYNC pulse of DACs output.
Output of CSYNC (pin 59): SYNC + 1 clock (see Figs 5 and 6).

Clock

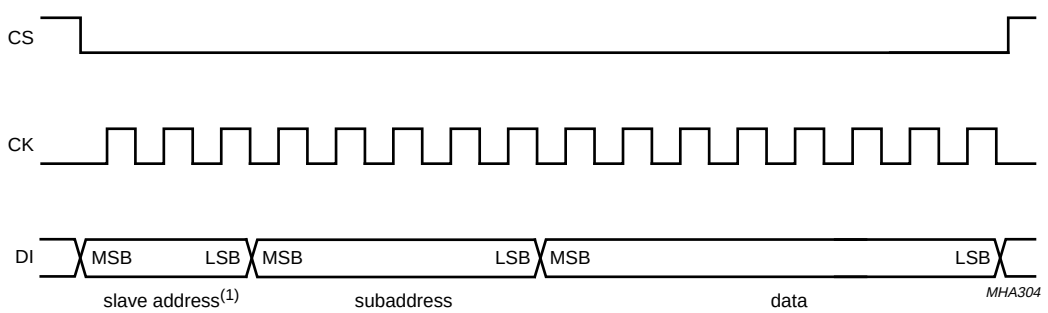
Table 1 Clock frequency

MODE	CCD	CLK1 (MHz)	CLK2 (MHz)
NTSC	510H	9.5350	19.0699
	670H	12.7132	–
	720H	13.5000	–
	768H	14.3182	–
PAL SECAM	510H	9.6563	19.3125
	670H	12.8750	–
	720H	13.5000	–
	768H	14.1875	–

Table 2 Clock used for each block

MODE	SSG BLOCK	Y/C BLOCK	ENCODER BLOCK	Y-DAC BLOCK	C-DAC BLOCK
510H NTSC/PAL	CLK1	CLK1	CLK1 and CLK2 (upsampling)	CLK1	CLK2
Other modes	CLK1	CLK1	CLK1	CLK1	CLK1

MICROPROCESSOR INTERFACE FORMAT



(1) Slave address 001.

Fig.7 Microprocessor interface format.

Table 3 Microprocessor interface format

FUNCTION	SUBADDRESS	DATA							
		MSB							LSB
Field delay	00000	X	–	–	–	–	–	–	FD
Title enable	00000	X	–	–	–	–	–	TE	–
Title polarity	00000	X	–	–	–	–	TP	–	–
False colour +6 dB	00000	X	–	–	–	FCU	–	–	–
UV +6 dB	00000	X	–	–	CUP	–	–	–	–
Y +6 dB	00000	X	–	YUP	–	–	–	–	–
Y clear	00000	X	YCL	–	–	–	–	–	–
HAP LOW clip	00001	X	X	HA5	HA4	HA3	HA2	HA1	HA0
VAP LOW clip	00010	X	X	VA5	VA4	VA3	VA2	VA1	VA0
AP HIGH clip	00011	X	–	–	–	AP3	AP2	AP1	AP0
AP gain	00011	X	AG2	AG1	AG0	–	–	–	–
Y gain	00100	X	X	YG5	YG4	YG3	YG2	YG1	YG0
Y pedestal	00101	YP7	YP6	YP5	YP4	YP3	YP2	YP1	YP0
Slice	00110	X	X	X	–	–	–	SLI	SNP
Mosaic	00110	X	X	X	MOS	PX1	PX0	–	–
Slice level	00111	SLL7	SLL6	SLL5	SLL4	SLL3	SLL2	SLL1	SLL0
Subcarrier	01000	S7	S6	S5	S4	S3	S2	S1	S0
	01001	S15	S14	S13	S12	S11	S10	S9	S8
	01010	–	–	–	–	S19	S18	S17	S16
UV polarity	01010	–	–	–	UVP	–	–	–	–
SYNCI	01010	–	–	SYN	–	–	–	–	–
Encoder mode	01010	EM1	EM0	–	–	–	–	–	–
Burst level	01011	X	BL6	BL5	BL4	BL3	BL2	BL1	BL0
HRST delay	01101	D7	D6	D5	D4	D3	D2	D1	D0
	01110	–	–	–	–	–	–	D9	D8
CCD type	01110	–	–	–	–	H1	H0	–	–
525/625 line	01110	–	–	–	LL	–	–	–	–
Master/slave	01110	–	–	MS	–	–	–	–	–
ADC delay	01110	AD1	AD0	–	–	–	–	–	–
Solarization	01111	X	X	X	–	–	–	TR1	TR0
	01111	X	X	X	–	–	SOL	–	–
Sepia	01111	X	X	X	–	SEP	–	–	–
Negative/positive	01111	X	X	X	NP	–	–	–	–
R gain	10000	X	RG6	RG5	RG4	RG3	RG2	RG1	RG0
B gain	10001	X	BG6	BG5	BG4	BG3	BG2	BG1	BG0
U gain	10010	X	X	UGP5	UGP4	UGP3	UGP2	UGP1	UGP0
	10011	X	X	UGN5	UGN4	UGN3	UGN2	UGN1	UGN0

FUNCTION	SUBADDRESS	DATA MSB							LSB
V gain	10100	X	X	VGP5	VGP4	VGP3	VGP2	VGP1	VGP0
	10101	X	X	VGN5	VGN4	VGN3	VGN2	VGN1	VGN0
U matrix 1 gain	10110	X	X	UM5	UM4	UM3	UM2	UM1	UM0
U matrix 2 gain	10111	X	X	UN5	UN4	UN3	UN2	UN1	UN0
V matrix 1 gain	11000	X	X	VM5	VM4	VM3	VM2	VM1	VM0
V matrix 2 gain	11001	X	X	VN5	VN4	VN3	VN2	VN1	VN0
SP polarity	11010	X	X	X	–	–	–	–	SPP
FH2 polarity	11010	X	X	X	–	–	–	FHP	–
Colour filter	11010	X	X	X	–	–	LPF	–	–
HD, VD polarity	11010	X	X	X	–	SHV	–	–	–
Sub LPF	11010	X	X	X	JGM	–	–	–	–
False colour	11011	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
White-clip level	11100	WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0
Y delay	11101	X	X	X	X	–	–	YDL1	YDL0
C delay	11101	X	X	X	X	CDL1	CDL0	–	–

Table 4 Explanation of functions of Table 3

SYMBOL	DESCRIPTION
FD	field delay control
TE	title enable control
TP	title polarity control
FCU	false colour plus 6 dB up
CUP	UV +6 dB up
YUP	Y gain +6 dB up
YCL	Y clear control
HA0 to HA5	horizontal aperture LOW clip level control
VA0 to VA5	vertical aperture LOW clip level control
AP0 to AP3	aperture HIGH clip level control
AG0 to AG2	aperture gain control
YG0 to YG5	Y gain control
YP0 to YP7	Y pedestal control
SNP	slice effect polarity
SLI	slice ON/OFF
PX0 and PX1	mosaic effect pixels control
MOS	mosaic ON/OFF
SLL0 to SLL7	slice level control
S0 to S19	subcarrier control
UVP	UV_{SEL} polarity control
SYN	SYNC signal selection

SYMBOL	DESCRIPTION
EM0 and EM1	encoder mode control
BL0 to BL6	burst level control
D0 to D9	HRST and VRST preset control
H0 and H1	CCD type selection
LL	525/625 line control
MS	master/slave control
AD0 and AD1	ADC delay control
TR0 and TR1	solarization effect control
SOL	solarization ON/OFF
SEP	sepia ON/OFF
NP	negative/positive ON/OFF
RG0 to RG6	red gain control
BG0 to BG6	blue gain control
UGP0 to UGP5	U gain control for positive side
UGN0 to UGN5	U gain control for negative side
VGP0 to VGP5	V gain control for positive side
VGN0 to VGN5	V gain control for negative side
UM0 to UM5	U matrix 1 gain control
UN0 to UN5	U matrix 2 gain control
VM0 to VM5	V matrix 1 gain control
VN0 to VN5	V matrix 2 gain control
SPP	SP polarity control
FHP	FH2 polarity control
LPF	colour filter control
SHV	HD and VD polarity control
JGM	sub LPF control for false colour
TH0 to TH7	threshold control for false colour suppression
WC0 to WC7	white-clip level control
YDL0 and YDL1	Y delay control
CDL0 and CDL1	C delay control

MICROPROCESSOR SETTING

Table 5 Field delay control

FIELD DELAY CONTROL	FD
Normal	0
One field delay	1

Table 6 Title enable control

TITLE ENABLE CONTROL	TE
Title insertion OFF	0
Title insertion ON	1

Table 7 Title polarity control

TITLE POLARITY CONTROL	TP
Negative	0
Positive	1

Table 8 False colour +6 dB up

FALSE COLOUR +6 dB UP	FCU
0 dB gain	0
+6 dB gain	1

Table 9 UV +6 dB up

UV +6 dB UP	CUP
0 dB gain	0
+6 dB gain	1

Table 10 Y gain +6 dB up

Y GAIN +6 dB UP	YUP
0 dB gain	0
+6 dB gain	1

Table 11 Y clear control

Y CLEAR CONTROL	YCL
Normal	0
Clear	1

Horizontal aperture LOW clip level control = HA5 to HA0.

Vertical aperture LOW clip level control = VA5 to VA0.

Aperture HIGH clip level control = AP3 to AP0.

$$\text{Aperture gain control} = \frac{AG[2:0]}{8}$$

$$\text{Y gain control} = \frac{YG[5:0]}{32}$$

Y pedestal level control = YP7 to YP0.

Table 12 Slice effect polarity

SLICE EFFECT POLARITY	SNP
Negative	0
Positive	1

Table 13 Slice ON/OFF

SLICE ON/OFF	SLI
OFF normal	0
ON slice	1

Table 14 Mosaic effect pixels control

MOSAIC EFFECT PIXELS CONTROL	PX1	PX0
4×4 pixels	0	0
8×8 pixels	0	1
16×16 pixels	1	0
32×32 pixels	1	1

Table 15 Mosaic ON/OFF

MOSAIC ON/OFF	MOS
OFF normal	0
ON mosaic	1

Slice level control = SLL7 to SLL0.

$$\text{Subcarrier frequency control} = \frac{S[19:0] \times f_{encoder}}{1048576}$$

Table 16 UV_{SEL} polarity control

UV_{SEL} POLARITY CONTROL	UVP
Normal	0 HIGH: U(B–Y) LOW: V(R–Y)
Invert	1 HIGH: V(R–Y) LOW: U(B–Y)

Table 17 SYNC signal selection

SYNC SIGNAL SELECTION	SYN
Internal SYNC	0
External SYNC (from SYNCI pin 60)	1

Table 18 Encoder mode control

ENCODER MODE CONTROL	EM1	EM0
PAL	0	0
NTSC	0	1
SECAM	1	0
Bypass	1	1

Burst level control $= \frac{BL\,[6:0]}{128}$ (of full-scale DAC output).

HRST and VRST preset control = D9 to D0, preset horizontal counter to count D9 to D0.

Table 19 CCD type selection

CCD TYPE SELECTION	H1	H0
510H	0	0
670H	0	1
720H	1	0
768H	1	1

Table 20 525/625 line control

525/625 LINE CONTROL	LL
525 line	0
625 line	1

Table 21 Master/slave control

MASTER/SLAVE CONTROL	MS
Master	0
Slave	1

Table 22 AD converter delay control

ADC DELAY CONTROL (CAMDSP DELAY)	AD1	AD0
3Ts	0	0
4Ts	0	1
5Ts	1	0
6Ts	1	1

Table 23 Solarization effect control

SOLARIZATION EFFECT CONTROL (SLICE OF BITS)	TR1	TR0
3 bits (LSB)	0	0
4 bits (LSB)	0	1
5 bits (LSB)	1	0
6 bits (LSB)	1	1

Table 24 Solarization ON/OFF

SOLARIZATION ON/OFF	SOL
Normal	0
Solarization ON	1

Table 25 Sepia ON/OFF

SEPIA ON/OFF	SEP
Normal	0
Sepia ON	1

Table 26 Negative/positive ON/OFF

NEGATIVE/POSITIVE ON/OFF	NP
Normal	1
Negative	0

$$\text{R channel gain control} = 1 + \frac{RG[6:0]}{128}\ (1)$$

$$\text{B channel gain control} = 1 + \frac{BG[6:0]}{128}\ (1)$$

$$\text{U gain control for positive side} = \frac{UGP[5:0]}{16}$$

$$\text{U gain control for negative side} = \frac{UGN[5:0]}{16}$$

$$\text{V gain control for positive side} = \frac{VGP[5:0]}{16}$$

$$\text{V gain control for negative side} = \frac{VGN[5:0]}{16}$$

$$\text{U matrix 1 gain control} = \frac{UM[5:0]}{32}\ (1)$$

$$\text{U matrix 2 gain control} = \frac{UN[5:0]}{32}\ (1)$$

$$\text{V matrix 1 gain control} = \frac{VM[5:0]}{32}\ (1)$$

$$\text{V matrix 2 gain control} = \frac{VN[5:0]}{32}\ (1)$$

Table 27 SP polarity control

SP POLARITY CONTROL	SPP	
Normal	0	H: Ye + Mg or Ye + Gr
		L: Cy + Gr or Cy + Mg
Invert	1	H: Cy + Gr or Cy + Mg
		L: Ye + Mg or Ye + Gr

Table 28 FH2 polarity control

FH2 POLARITY CONTROL	FHP	
Normal	0	H: 2B-G
		L: 2R-G
Invert	1	H: 2R-G
		L: 2B-G

Table 29 Colour filter control

COLOUR FILTER CONTROL	LPF	
LPF1	0	[1,1,3,3,4,4,4,4,3,3,1,1]/32
LPF2	1	[–1,0,4,8,10,8,4,0,–1]/32

Table 30 HD and VD polarity control

HD AND VD POLARITY CONTROL	SHV
Normal	0
Invert	1

Table 31 Sub LPF control for false colour

SUB LPF CONTROL FOR FALSE COLOUR	JGM
Normal	0
Sub LPF	1

Threshold control for false colour suppress = TH7 to TH0.

White clip level control = 2 × WC7 to WC0.

Table 32 Y delay control

Y DELAY CONTROL	YDL1	YDL0
0 clock period	0	0
+1 clock period	0	1
+2 clock periods	1	0
+3 clock periods	1	1

Table 33 C delay control

C DELAY CONTROL	CDL1	CDL0
0 clock period	0	0
+1 clock period	0	1
+2 clock periods	1	0
+3 clock periods	1	1

(1) RG, BG, UM, UN, VM and VN are twos complement.

CAMERA

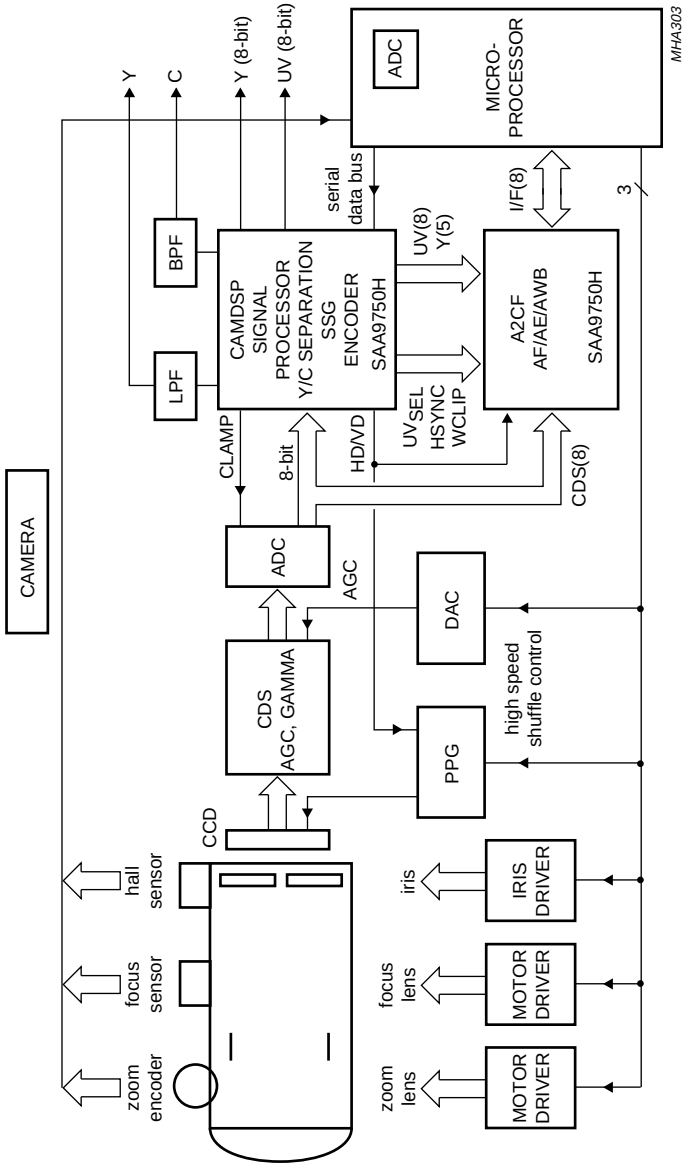
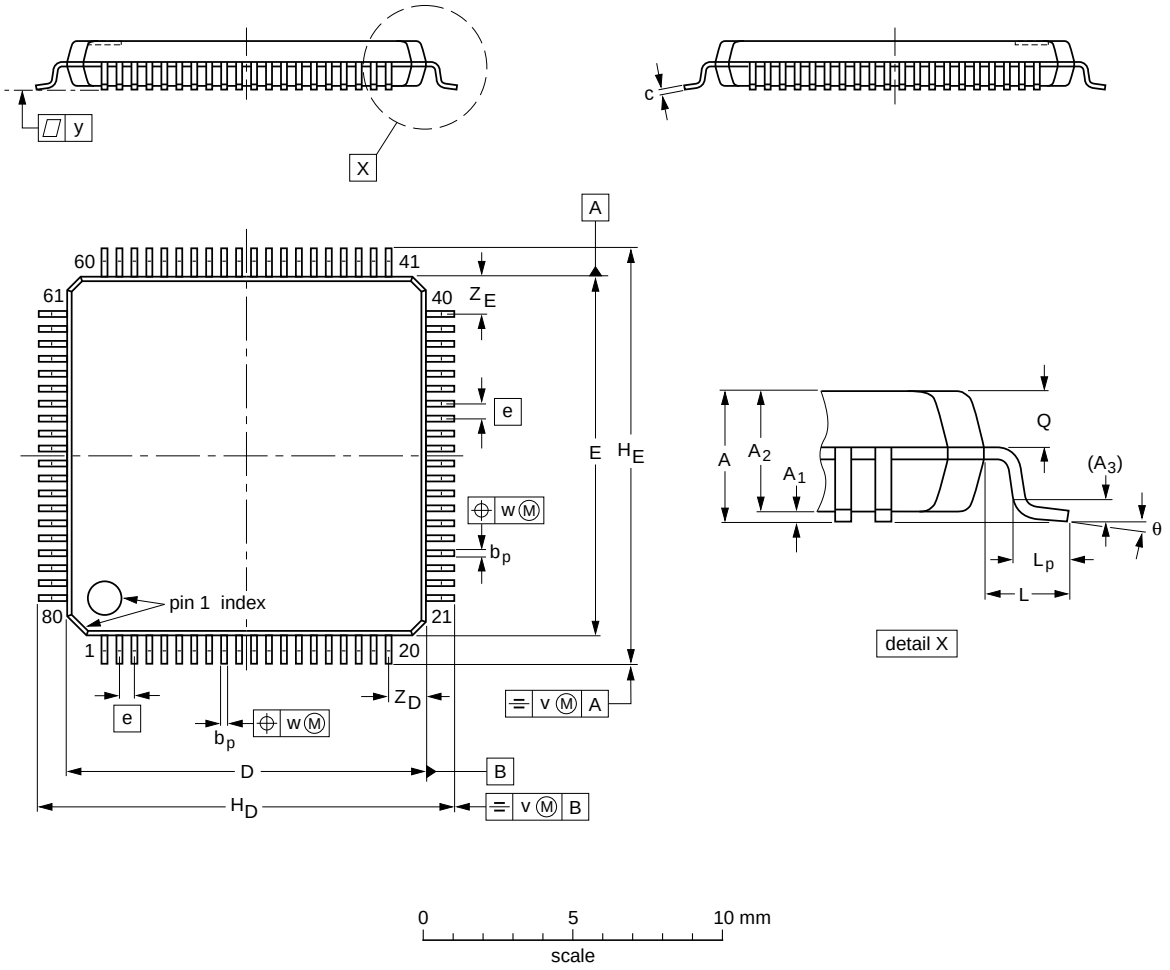


Fig.8 Camera block diagram (SAA9750H and SAA9740H).

PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.25 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1.0	0.7 0.3	0.70 0.58	0.2	0.15	0.1	1.45 1.05	1.45 1.05	4^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT315-1						~~92-03-24~~ 95-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
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